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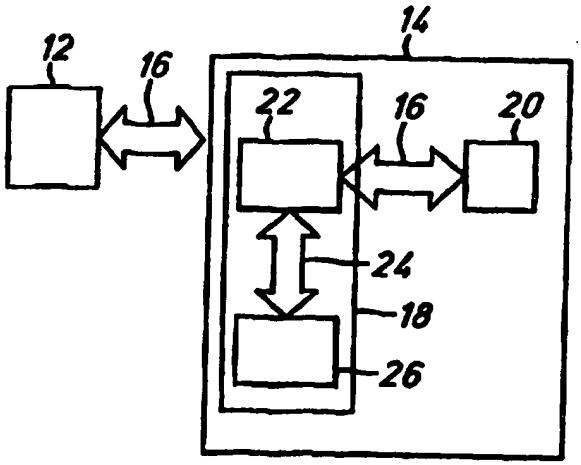
(57) Abstract

A data storage arrangement for a host computer or the like (12) with a relatively slow-access mass data storage device (20) such as a magnetic disc unit has relatively fast-access data store (26) consisting, at least in part, of non-volatile memory and a controller means (22) connectible as part of the computer's address space to act as a cache to speed access to the mass storage device.



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Memory Device

The present invention relates to memory devices. It finds particular application in the field of data storage in computers.

Computer systems rely on storage areas to save data which is necessary for executing programs, archiving, and other purposes. These storage areas (sometimes called mass storage areas) must be able to store data even when no power is applied to the computer, so that the data can be retrieved at some later time when power is reapplied. Thus a non-volatile storage medium is required. One common non-volatile storage medium is the magnetic disk drive, another non-volatile storage medium is a solid state disk that emulates magnetic disk drives.

These storage media have disadvantages associated with them. One disadvantage of magnetic disks is that the access time is comparatively slow because of the seek latency and rotational latency of the electro-mechanical disk drive. Solid state disks can be accessed much faster than magnetic disks, but even solid state disks can suffer from poor performance. For example, FLASH EPROM is frequently used in solid state disk applications because each cell is small so the storage density is high. However, FLASH EPROM is only block erasable, and erasure of a block of cells can take a number of seconds.

To overcome the problems of slow write and erase times, caches are sometimes used. A cache is usually a volatile memory which stores the most recent data accessed by the host. When power to the memory system is removed the data in the cache is copied to the mass storage device. The advantage of a cache is that it enables a large, slow memory to appear as a large, fast memory by adding a small fast memory.

Cache memory operates under the control of a cache manager which ensures that appropriate data is always accessible in the cache. One disadvantage of a cache is that the algorithms used by the cache manager are often very complicated so a cache is usually designed to work with a particular system and requires a large processing overhead.

One other form of cache is a software cache. A software cache is implemented by the processor of a computer. The processor uses the memory of the computer as a cache and it also uses an area of the storage medium in use to store data blocks as they are transferred to and from the cache.

According to the present invention there is provided data storage arrangement for a host computer or the like having a relatively slow-access mass data storage device connected thereto wherein said data storage arrangement comprises relatively fast-access data storage means consisting, at least in part, of non-volatile memory and controller means connectible to said host computer and to said mass data storage device, selectively to route data between said host computer and either said mass data storage device or said relatively fast-access data storage means.

The present invention relates to a system that can be inserted into a standard personal computer, or other data processing device, and connected to a standard storage medium such as a magnetic disk. The system uses fast non-volatile memory to provide permanent storage of data and it may also incorporate some fast memory to act as a data buffer, thus increasing the performance of the storage medium that is being used.

The present invention differs from a software cache in a number of ways. It relates to hardware which can be connected to existing hardware to provide a cache-like function with permanent storage of the information. Since most caches are volatile, the contents of a cache must be generated over a period of time. Thus, the initial access of each data entry in the cache must be to the mass storage device. The high speed memory of the present invention is located entirely in the mass storage device: no executable code is required to occupy valuable main memory space.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made by way of example to the accompanying drawing in which:

Figure 1 shows a diagram of a computer system;

Figure 2 shows a diagram of a master-slave memory system;

Figure 3 shows a diagram of a master-slave memory system showing detail of the master unit;

Figure 4 shows a diagram of a high speed memory; and

Figure 5 shows a diagram of an implementation of the present invention.

Figure 1 shows a typical arrangement for a computer system 10 where a host 12 (such as a personal computer) is connected to a memory system 14 by a standard interface 16. The standard interface could be such as is conventionally used with a magnetic disk,

for example an ATA or an IDE interface). The memory system 14 stores data which is accessed by the host 12 via the standard interface 16.

The memory system 14 shown in Figure 1 is composed of a master unit 18 and a slave unit 20 connected by a standard interface 16. This is shown in Figure 2. The slave unit 20 is typically a magnetic disk which serves as the high volume storage area (the mass storage area) for storing information sent by the host 12.

The memory system 14 provides the same function to the host 12 as would be provided if the slave unit 20 was connected directly to the host 12. That is, the existence of the master-slave arrangement is transparent to the host 12.

The master unit 18 is a high speed, non-volatile memory system which comprises a controller 22, a first internal interface 24 and a high speed memory 26. The first internal interface 24 may be the same as the standard interface 16.

The master unit 18 forms a portable store which can be connected to any standard magnetic disk and appropriate standard interface 16 to improve access to the magnetic disk. The non-volatile memory capacity of the memory system 14 is the sum of the capacities of the master unit 18 and the slave unit 20.

The function of the controller 22 within the master unit 18 is to ensure that a high proportion of the data sector accesses made by the host 12 are made to the high speed memory 26 rather than the slave unit 20. This provides a higher performance than if the slave unit 20 is always accessed. The controller 22 also maintains a lookup table that stores the location of each data sector, for example, whether a data sector is in the high speed memory 26 or in the slave unit 20.

The controller 22 ensures that a high proportion of the data accesses requested by the host 12 are in the high speed memory 26 by relocating data sectors between the high speed memory 26 and the slave unit 20.

Sectors written by the host 12 would normally be located in the high speed memory 26: sectors read from the slave unit 20 would normally be simultaneously relocated to high speed memory 26. The controller 22 would normally also have access to the host's File Allocation Table (FAT) and could relocate sectors which are part of an active file (a file currently being used). Other techniques used in conventional cache memories could also be applied to the present invention.

In some embodiments of the present invention multiple high speed memories 26 may also be connected to a single controller 22.

The memory system of the present invention differs from a conventional cache memory in that both the high speed memory 26 and the slave unit 20 are non-volatile memories. Data is not temporarily located in the high speed memory 26 as a copy of the data in the slave unit 20, as is the case with a high speed cache. Only one version of each data sector is maintained. The data sector is stored either in the high speed memory 26 or in the slave unit 20. Thus the memory configuration is retained when electrical power is restored.

One of the characteristics of the present invention is that it is configured as a single device conforming to a mass storage standard and occupying two physical disk slots. In some embodiments of the present invention multiple slave units 20 are connected to a single master unit 18.

In another embodiment of the present invention the high speed memory 26 comprises two memories: a non-volatile memory 28 and a volatile memory 30 connected by a second internal interface 32. The second internal interface 32 could be identical to the first internal interface 24 or it may conform to a different standard. The volatile memory 30 is used as a buffer memory to allow fast write operations. In this embodiment the volatile memory 30 is a Static Random Access Memory (SRAM) and the non-volatile memory 28 is a FLASH EPROM. All data sectors stored in the SRAM 30 will be copied to the FLASH EPROM 28 for permanent storage.

Typically, the FLASH EPROM 28 will have some means of ensuring uniform memory usage to avoid excessive wear of the FLASH EPROM cells, this function may be implemented by a high speed memory control unit 34. Since FLASH EPROM 28 has a slow write cycle, the SRAM 30 is used to improve the performance of the master unit 18 for writing data.

If the high speed memory 26 had a fast access time and a fast write/erase cycle then the high speed memory control unit 34 would not need any additional memory, because the memory is used as a buffer for the solid state disk.

The controller 22 also has the necessary logic to move data from the high speed memory 26 to the slave unit 20 to liberate space in the high speed memory as the free space

in the high speed memory 26 diminishes. The movement of data between the high speed memory 26 and the slave unit 20 is controlled by the controller 22. Numerous algorithms exist for determining when data should be relocated from one area of memory to another. For example, some algorithms ensure that the data sector which was accessed least recently is moved from the cache to the mass storage area first. Other algorithms relocate the sector that is accessed least frequently first. The present invention is suitable for use with any convenient algorithm.

It will be appreciated that various modifications may be made to the above described embodiment within the ambit of the present invention. For example, although a magnetic disk was described in the embodiment, the invention could also be used with a holographic memory, a ferro-electric memory or any convenient memory medium.

Claims

1. A data storage arrangement for a host computer or the like (12) having a relatively slow-access mass data storage device (20) connected thereto **characterised in that** said data storage arrangement comprises relatively fast-access data storage means (26) consisting, at least in part, of non-volatile memory and controller means (22) connectible to said host computer and to said mass data storage device, selectively to route data between said host computer (12) and either said mass data storage device (20) or said relatively fast-access data storage means (26).

2. A data storage arrangement for a host computer or the like according to claim 1 **characterised in that** said relatively fast-access data storage means (26) further includes relatively fast-access volatile memory (30) to act as a data buffer, thereby increasing the performance of the storage medium that is being used.

3. A data storage arrangement for a host computer or the like according to claim 2 **characterised in that** said volatile memory (30) comprises Static Random Access Memory.

4. A data storage arrangement for a host computer or the like according to claim 1 **characterised in that** said relatively fast-access data storage means (26) comprises FLASH erasable programmable read-only memory.

5. A data storage arrangement for a host computer or the like according to claim 4 **characterised in that** said relatively fast-access data storage means (26) includes means (34) adapted to equalise usage of said erasable programmable read-only memory.

6. A data storage arrangement for a host computer or the like according to claim 4 **characterised in that** said relatively fast-access data storage means (26) includes static random-access memory (30) to improve the speed of access of said host computer or the like for writing data.

7. A data storage arrangement for a host computer or the like according to claim 1 **characterised in that** said controller means (22) includes logical circuit arrangements to ensure that a greater proportion of data sector accesses made by the host (12) are to the

relatively fast access data storage means (26) rather than the mass data storage device (20).

8. A data storage arrangement for a host computer or the like according to claim 1 **characterised in that** said controller means (22) includes storage means to store information on whether a data sector is currently in said relatively fast-access data storage means (26) or in the mass data storage device (20).

9. A data storage arrangement for a host computer or the like according to claim 7 **characterised in that** said controller means (22) includes means to relocate data between said relatively fast access data storage means (26) and said mass data storage device (20).

10. A data storage arrangement for a host computer or the like according to claim 9 **characterised in that** said controller means (22) includes means to relocate data between said relatively fast access data storage means (26) and said mass data storage device (20) by ensuring that the data sector which was accessed least recently is moved from the cache to the mass storage area first.

11. A data storage arrangement for a host computer or the like according to claim 9 **characterised in that** said controller means (22) includes means to relocate data between said relatively fast access data storage means (26) and said mass data storage device (20) by ensuring that the data sector which is accessed least frequently is moved from the cache to the mass storage area first.

12. A demountable data storage arrangement for a host computer or the like according to any one of the preceding claims **characterised in that** it has an input and an output interface having a common format whereby it may be interposed between said host computer (12) and said mass data storage device (20).

13 A computer system incorporating a data storage arrangement in accordance with any one of the preceding claims.

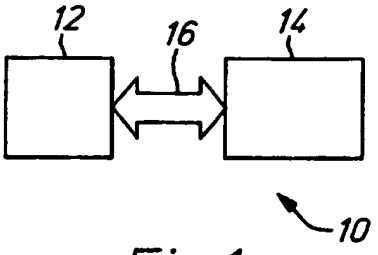

Fig.1

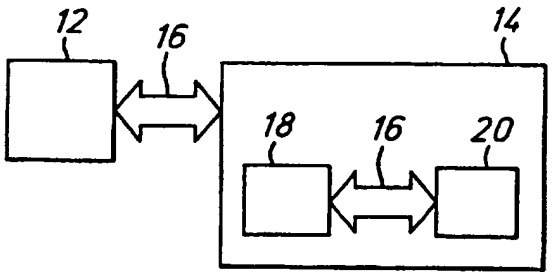

Fig.2

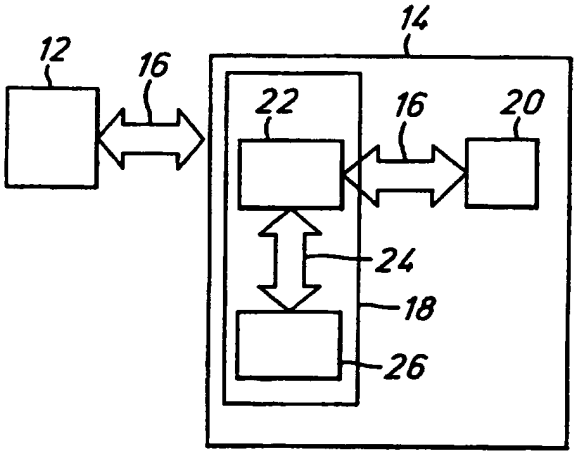

Fig.3

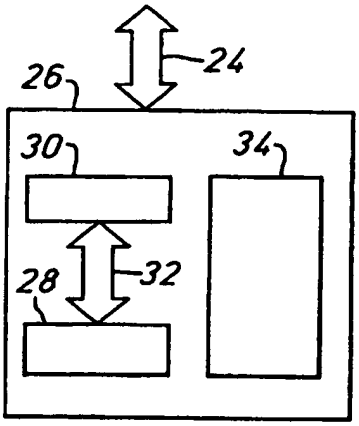

Fig.4

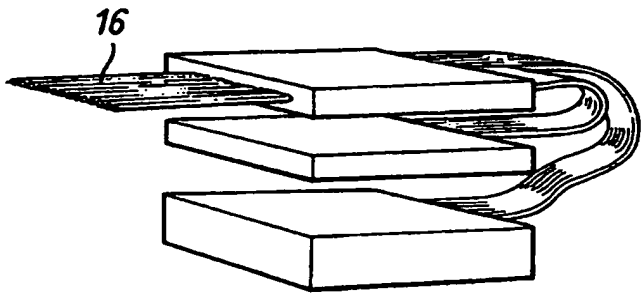

Fig.5

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/GB 97/01532

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F12/08 G06F3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 564 699 A (FUJITSU LTD) 13 October 1993 see column 2, line 50 - column 3, line 18 see column 4, line 22 - line 26 see column 5, line 49 - column 6, line 22 see figure 1 ---	1,2,4,5, 7-10,12, 13
Y	EP 0 702 305 A (NIPPON ELECTRIC CO) 20 March 1996 see abstract see column 1, line 36 - line 38 see column 3, line 44 - line 47 see column 4, line 27 - line 37 see column 11, line 12 - line 40 see figure 1 --- -/--	1,2,4,5, 7-10,12, 13

[X] Further documents are listed in the continuation of box C.

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 522 780 A (IBM) 13 January 1993	5
A	see column 9, line 22 - line 29	4
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